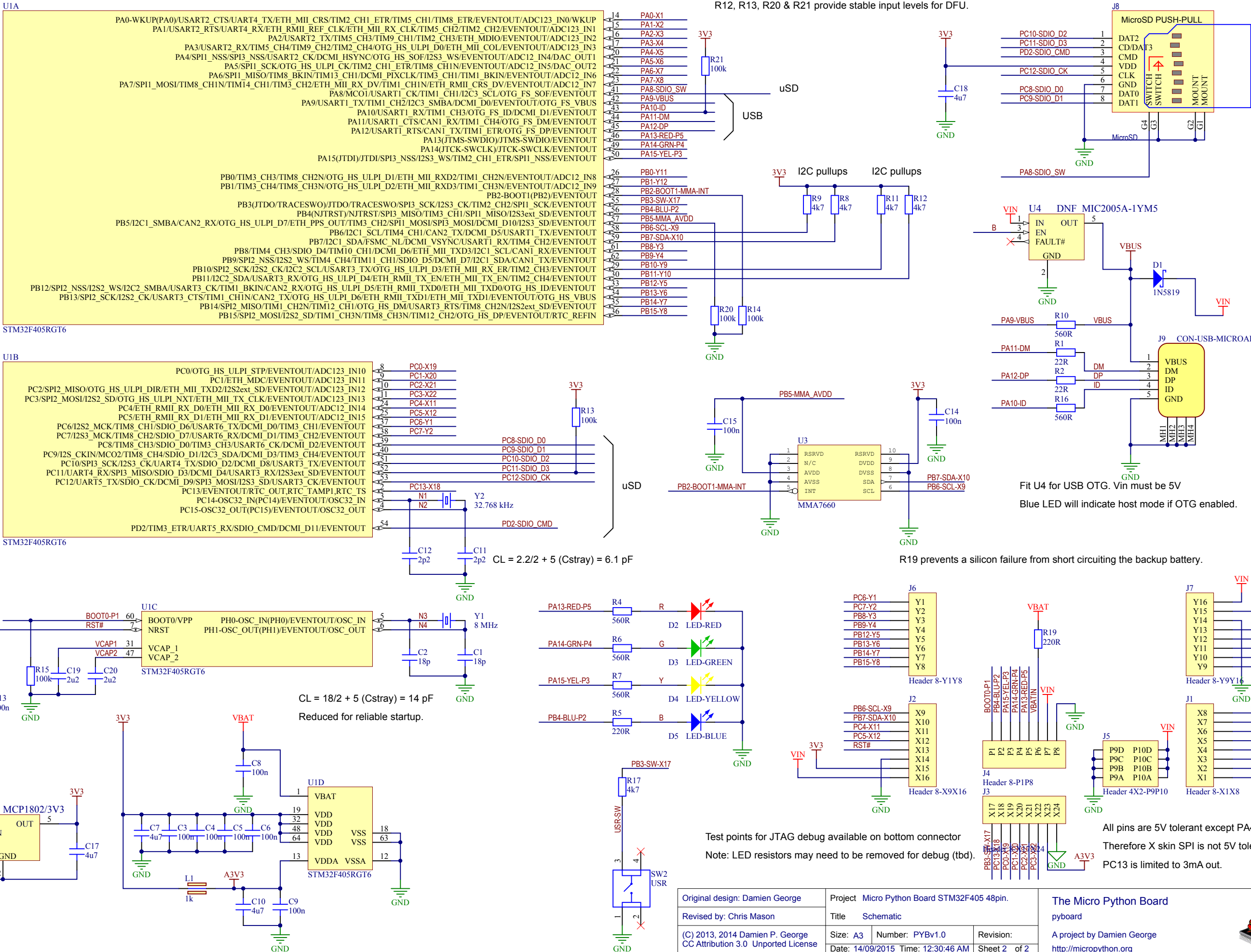


USB DFU requires stable levels on PA10, PB5, PB11 & PC11. PB2 must be low during boot.

R12, R13, R20 & R21 provide stable input levels for DFU.



Note: Functions marked * are standardised symmetrical functions (except CAN1**).

PB6/7 and PB10/11 are extra symmetrical Serial ports for F405 module.

Not available on CPUs with 2 serial ports.

Other functions may not be available with different CPUs

1.3in x 1.65in 33mm x 42mm

Internal use ports

PA9/OTG-VBUS

PA10/OTG-ID

PA11/USB-DM

PA12/USB-DP

PC8/SDIO_D0

PC9/SDIO_D1

PC10/SDIO_D2

PC11/SDIO_D3

PC12/SDIO_CLK

PA8/SDIO_SW

PD2/SDIO_CMD

PB6/SCL/MMA-SCL (shared with pin)

PB7/SDA/MMA-SDA (shared with pin)

PB2/BOOT1//MMA_INT

PB5/MMA_AVDD

PB4/BLE_LED/JTAG-TRST (shared with pin)

PA13/RED_LED/JTAG-TMS/SWDIO (shared with pin)

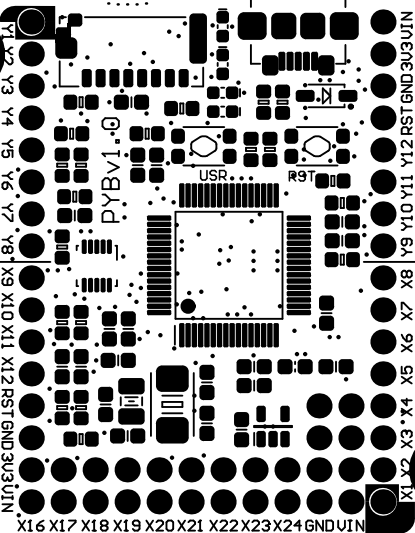
PA14/GRN_LED/TCK/SWCLK (shared with pin)

PA15/YEL_LED/TDI (shared with pin)

PB3/USR_SW/TDO/TRACESW0 (shared with pin)

PC6/TX6*/PWM* Y1
PC7/RX6*/PWM* Y2
PB8/CANRX1**/PWM* Y3
PB9/CANTX1**/PWM* Y4
PB12/SS2*/CANRX2 Y5
PB13/SCK2*/CANTX2/PWM Y6
PB14/MISO2*/PWM Y7
PB15/MOSI2*/PWM Y8
PB6/SCL1*/4k7PU/TXD1/PWM X9
PB7/SDA1*/4k7PU/RXD1/PWM X10
PC4/ADC* X11
PC5/ADC* X12
RST* X13
GND X14
3V3 X15
VIN X16

Y16 VIN
Y15 3V3
Y14 GND
Y13 RST*
Y12 PB1/ADC*/PWM
Y11 PB0/ADC*/PWM
Y10 PB11/SDA2*/4k7PU/RX3/PWM
Y9 PB10/SCL2*/4k7PU/TX3/PWM
X8 PA7/MOSI1*/ADC/PWM
X7 PA6/MISO1*/ADC/PWM
X6 PA5/SCK1*/ADC/DAC/PWM (3V3)
X5 PA4/SS1*/ADC/DAC (3V3)
X4 PA3/RX2/ADC/PWM*/SERVO
X3 PA2/TX2/ADC/PWM*/SERVO
X2 PA1/RX4*/ADC/PWM*/SERVO
X1 PA0/TX4*/ADC/PWM*/SERVO



INNER ROW (P)

OUTER ROW (X)

PB3/USR_SW/TDO	BOOT0	P1
PC13<3mA>	PB4/BLU_LED/TRST	P2
PC0/ADC	PA15/YEL_LED/TDI	P3
PC1/ADC	PA14/GRN_LED/TCK	P4
PC2/ADC	PA13/RED_LED/TMS	P5
PC3/ADC	UBAT	P6
A3V3	VIN	P7
A6ND	GND	P8
	SERVO	P9A-D
	SERVO	P10A-D
	VIN	

DESIGN RULES.

Board profile and connector grid. 1.27mm (50mil).

Component placement grid. 0.25mm

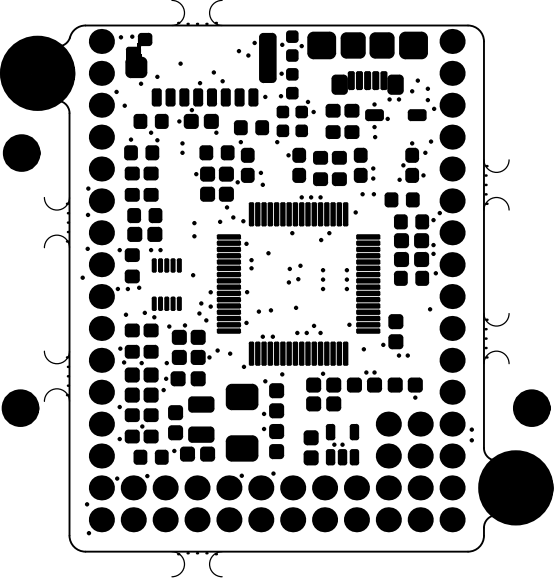
Routing grid. 0.05mm

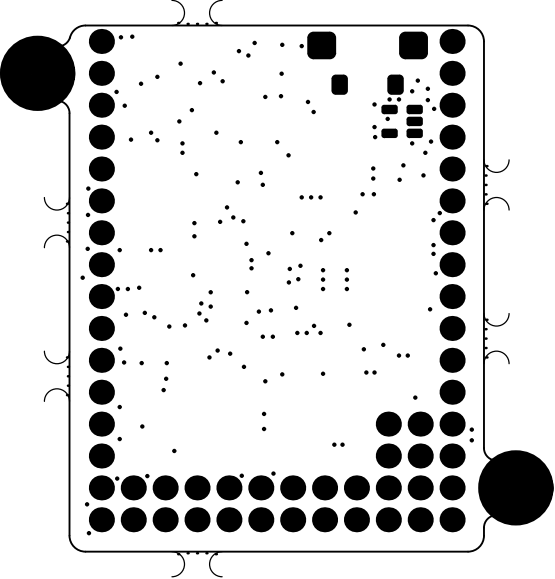
Minimum track and spacing. 0.15mm (6mil).

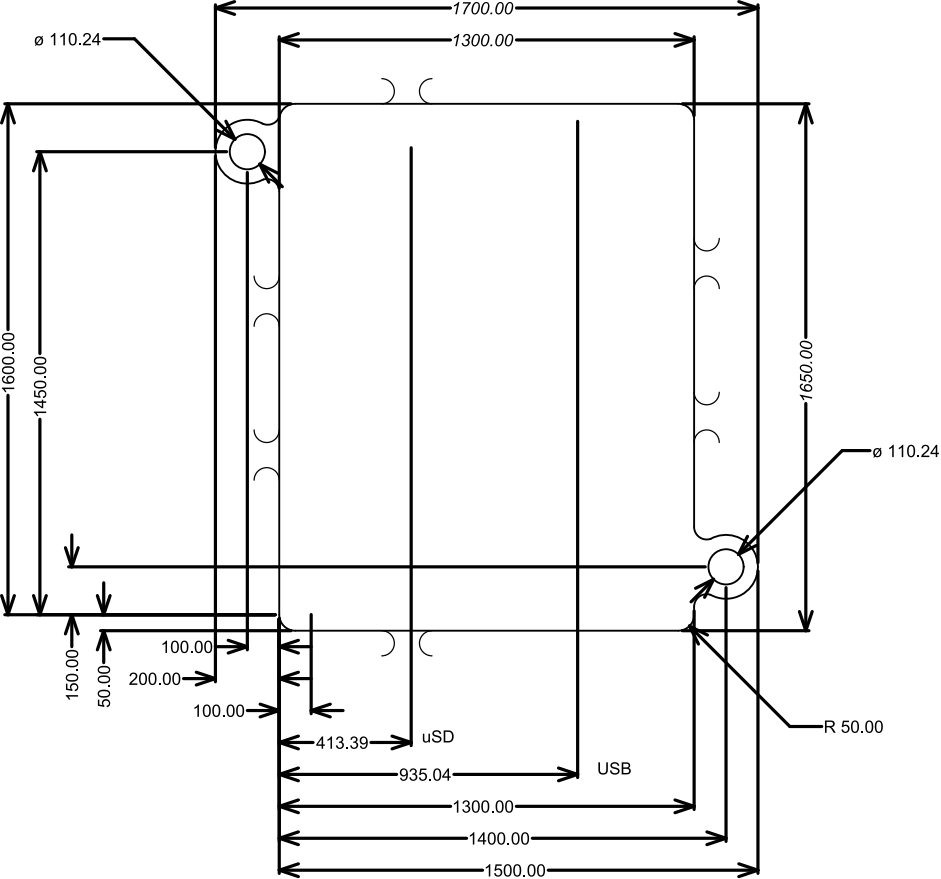
Minimum via size. Hole 0.25mm, pad 0.6mm.

PCB spec.

2 layer 1.6mm FR4. Green mask. White legend - 2 sides. Gold finish pb free. Electrical te



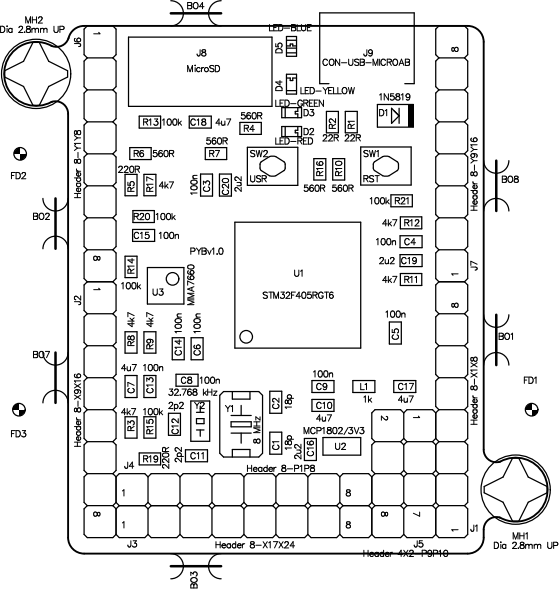




The board origin (0,0) is the bottom left corner of a half size skin compatible with X or Y position.

The pyboard extends 1.27mm (50mil) below the origin to allow for labels on the bottom connector.

Dimensions in italics are for reference only.





DNF MIC2005A-1YM5

