USB DFU requires stable levels on PA10, PB5, PB11 & PC11. PB2 must be low during boot.

R12, R13, R20 & R21 provide stable input levels for DFU.

U1A

STM32F405RGT6

U1B

STM32F405RGT6

uSD

USB

I2C pullups

I2C pullups

MicroSD PUSH-PULL

Fit R16 & R18 for USB OTG. Vin must be 5V

R19 prevents a silicon failure from short circuiting the backup battery.

U1C

STM32F405RGT6

U1D

STM32F405RGT6

U2 MCP1802/3V3

U3

MMA7660

Test points for JTAG debug

rest of JTAG & SW debug available on bottom connector

Note: LED resistors may need to be removed for debug (tbd).

Original design: Damien George	Project Micro Python Board STM32F405 40pin.		The Micro Python Board
Revised by: Chris Mason	Title Schematic		pyboard
(C) 2013, 2014 Damien P. George CC Attribution 3.0 Unported License	Size: A3	Number: PYBv4	Revision:	A project by Damien George
	Date: 6/01/2014 Time: 8:11:14 AM	Sheet 2 of 2		http://micropython.org
File: L:\ NEW Projects\MICRO PYTHON\PYBv4dev\PYBv4-sh2.SchDoc			

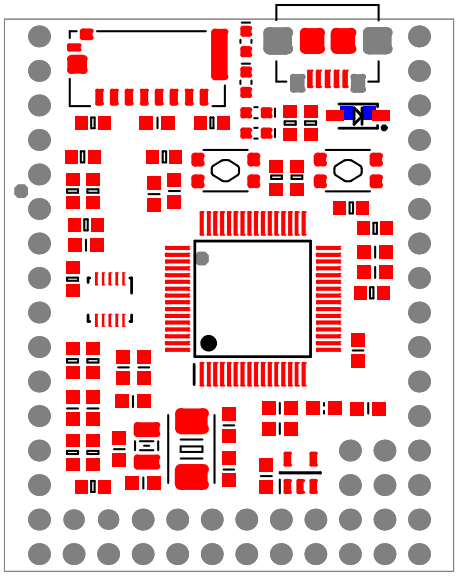
Note: Functions marked * are standardised symetrical functions (except CAN1**).

PB6/7 and PB10/11 are extra symetrical Serial ports for F405 module.

Not available on CPUs with 2 serial ports.

Other functions may not be available with different CPUs

1.3in x 1.6in 33mm x 40.6mm



PC6/TX6*/PWM*	Y9	Y8	VIN	PA9/OTG-VBUS
PC7/RX6*/PWM*	Y10	Y7	3V3	PA10/OTG-ID
PB8/CANRX1**/PWM*	Y11	Y6	GND	PA11/USB-DM
PB9/CANTX1**/PWM*	Y12	Y5	RST*	PA12/USB-DP
PB12/SS2*/CANRX2	Y13	Y4	PB1/ADC*/PWM	PC8/SDIO_D0
PB13/SCK2*/CANTX2/PWM	Y14	Y3	PB0/ADC*/PWM	PC9/SDIO_D1
PB14/MISO2*/PWM	Y15	Y2	PB11/SDA2*/4k7PU/RX3/PWM	PC10/SDIO_D2
PB15/MOSI2*/PWM	Y16	Y1	PB10/SCL2*/4k7PU/TX3/PWM	PC11/SDIO_D3
PB6/SCL1*/4k7PU/TXD1/PWM	X1	X16	PA7/MOSI1*/ADC/PWM	PC12/SDIO_CK
PB7/SDA1*/4k7PU/RXD1/PWM	X2	X15	PA6/MISO1*/ADC/PWM	PC13/SDIO_SW
PC4/ADC*	X3	X14	PA5/SCK1*/ADC/DAC/PWM	PD2/SDIO_CMD
PC5/ADC*	X4	X13	PA4/SS1*/ADC/DAC	PB6/SCL/MMA-SCL (shared with pin)
RST*	X5	X12	PA3/RX2/ADC/PWM*/SERVO	PB7/SDA/MMA-SDA (shared with pin)
GND	X6	X11	PA2/TX2/ADC/PWM*/SERVO	PB2/BOOT1//MMA_INT
3V3	X7	X10	PA1/RX4*/ADC/PWM*/SERVO	PB5/MMA_AVDD
VIN	X8	X9	PA0/TX4*/ADC/PWM*/SERVO	PB4/BLUE_LED/JTAG-TRST
				PA13/RED_LED/JTAG-TMS/SWDIO (shared with pin)
				PA14/GRN_LED/TCK/SWCLK (shared with pin)
				PA15/YEL_LED/TDI
				PB3/USR_SW/TDO/TRACESWO (shared with pin)

X17 P1	X18 P2	X19 P3	X20 P4	X21 P5	X22 P6	X23 P7	X24 P8	P9A-D	P10A-D	
3V3	BOOT0			VBAT	GND	VIN	GND			
PB3/USR_SW/TRACESWO	PC13	PC0/ADC	PC1/ADC	PC2/ACD	PC3/ADC	A3V3	AGND	SERVO GND	SERVO VIN	
		PA13/RED_LED/SWDIO	PA14/GRN_LED/SWCLK							

DESIGN RULES.

Board profile and connector grid. 1.27mm (50mil).

Component placement grid. 0.25mm

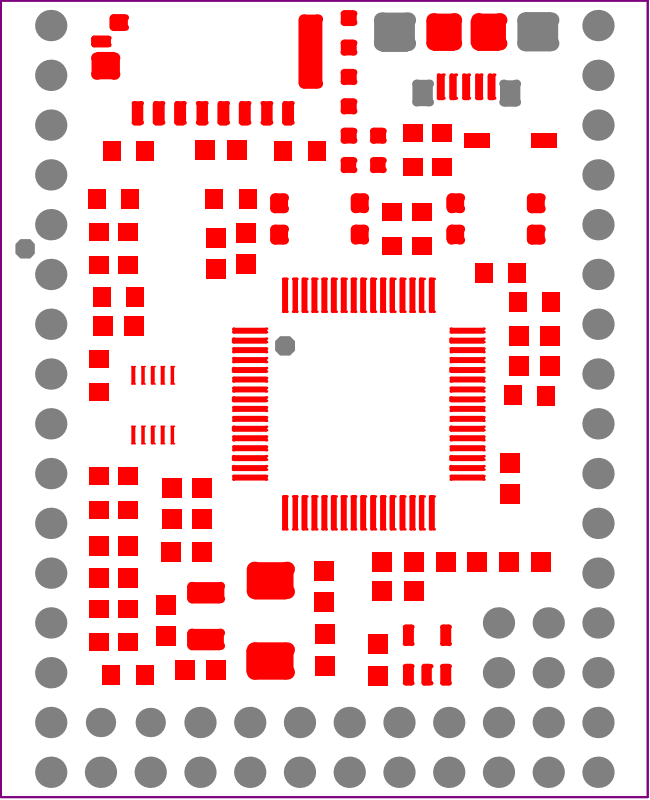
Routing grid. 0.05mm

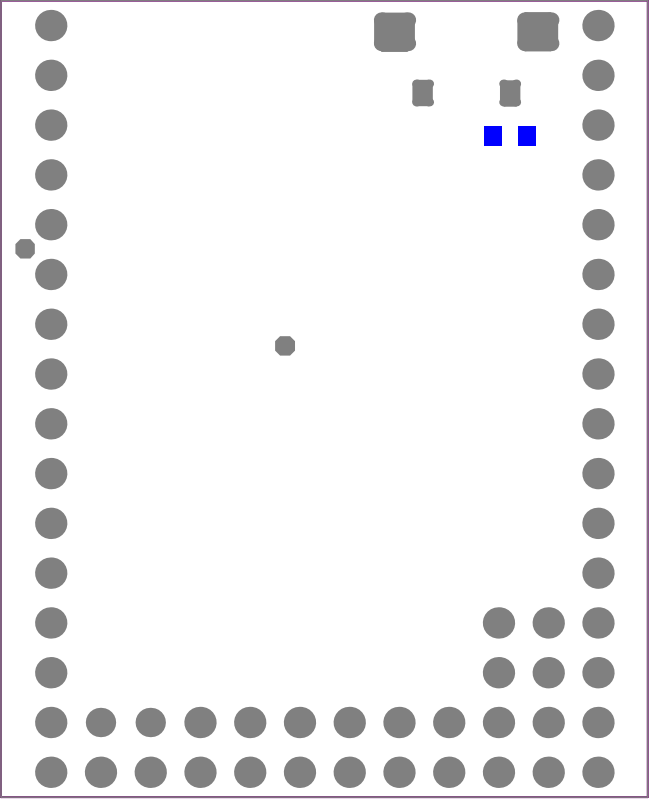
Minimum track and spacing. 0.15mm (6mil).

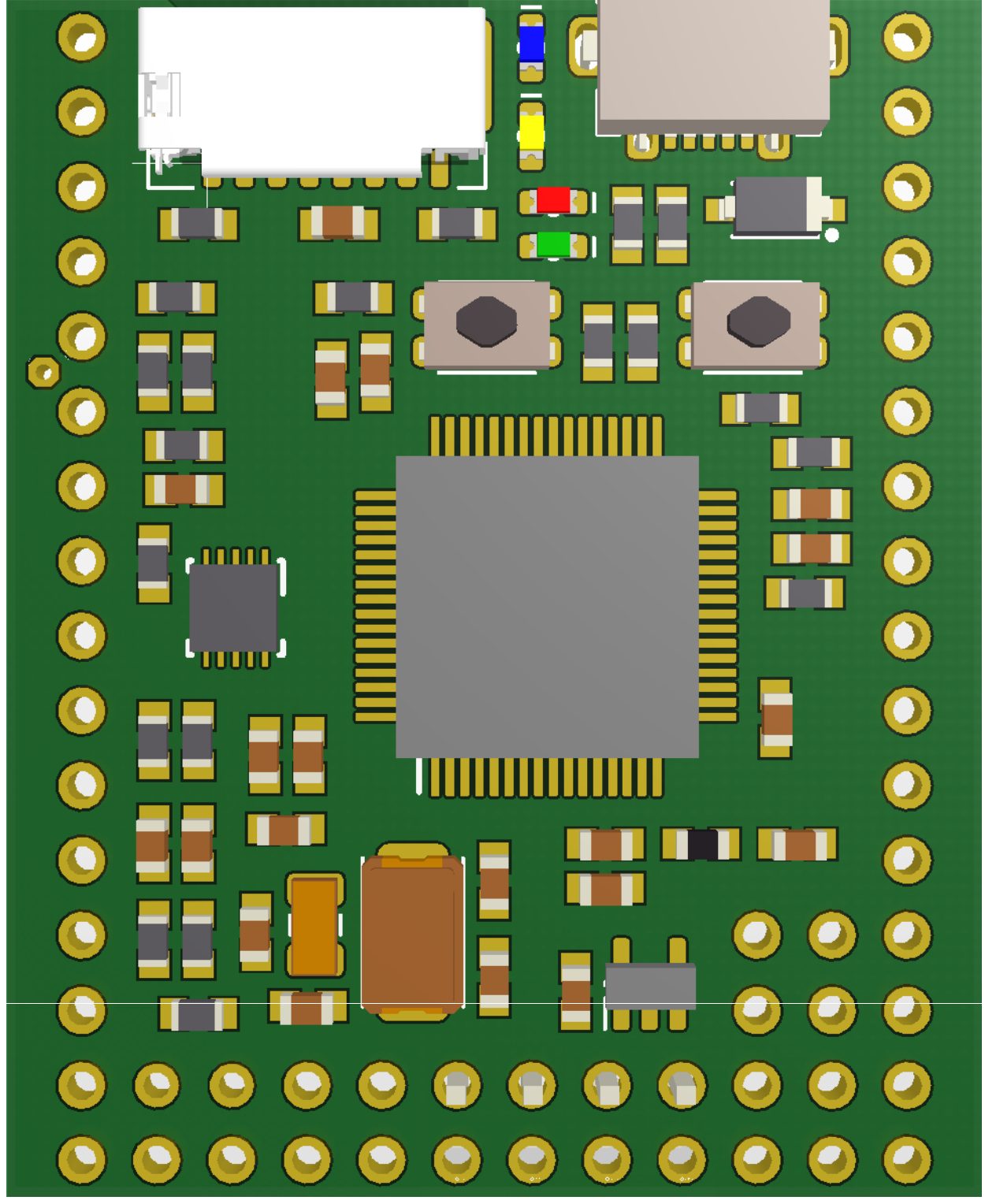
Minimum via size. Hole 0.25mm, pad 0.55mm (0.15mm annular ring).

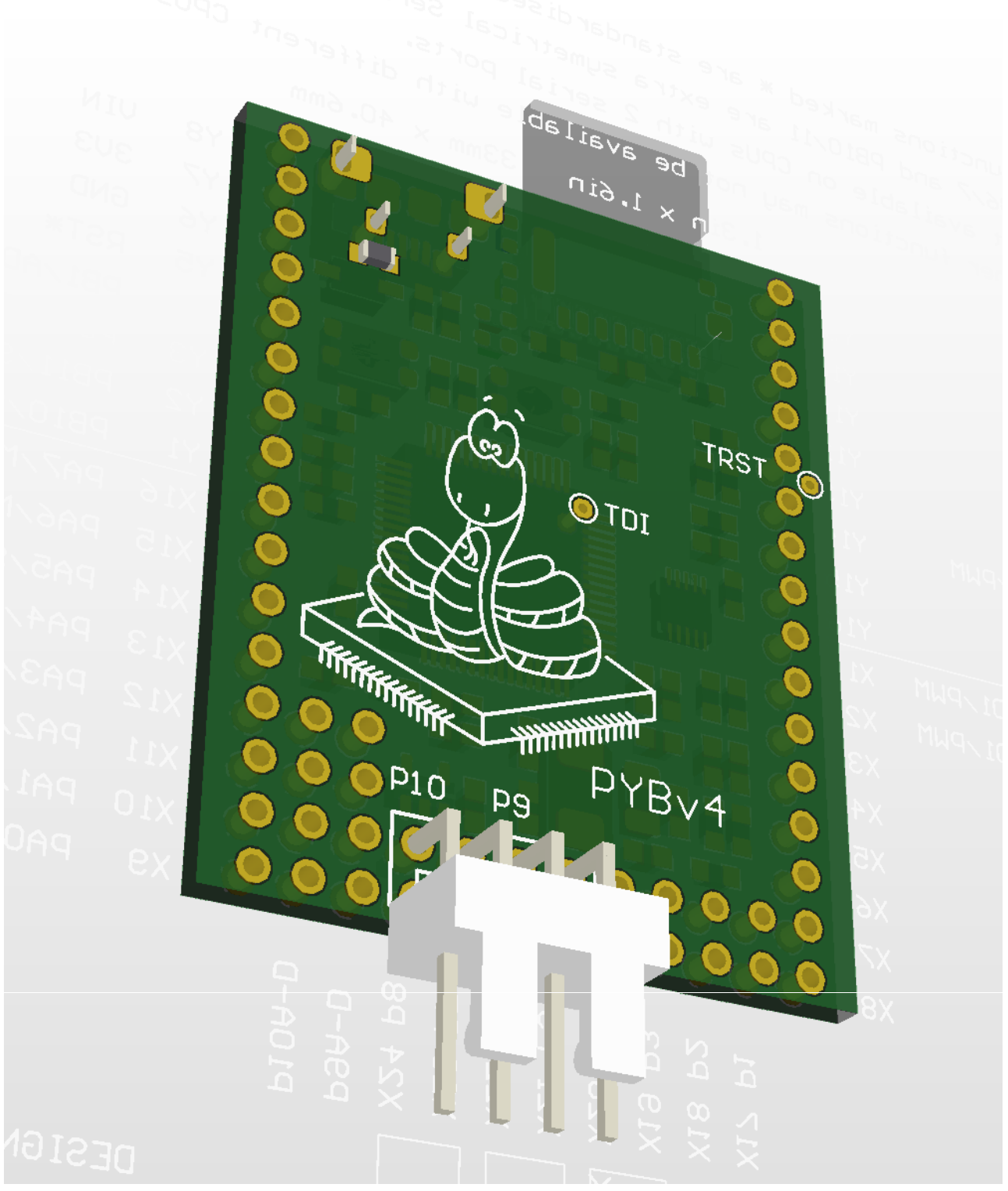
PCB spec.

2 layer 1.6mm FR4. Green mask. White legend - 2 sides. ENIG finish. Electrical test.








TRST
TDI
P10
P9
PYBv4